

ring, wherein the cover plate is adhesively coupled to the top surface of the semiconductor by a first adhesive, wherein the cover plate is adhesively coupled to a top surface of the stiffener ring by a second adhesive, and wherein an elastic modulus of the first adhesive is less than an elastic modulus of a second adhesive.

The present invention provides an electronic structure, comprising:

- a substrate;
- a semiconductor electrically coupled to the substrate; and
- a cover plate on a top surface of the semiconductor, wherein the cover plate is adhesively coupled to the top surface of the semiconductor by a first adhesive, and wherein the first adhesive has an elastic modulus less than about 500 psi.

The present invention provides a method for forming an electronic structure, comprising :

- providing a semiconductor device;
- electrically coupling the semiconductor device to a substrate;
- adhesively coupling a stiffener ring to the substrate, wherein the stiffener ring surrounds the semiconductor device, and
- adhesively coupling a cover plate to a top surface of the semiconductor device with a first adhesive and to a top surface of the stiffener ring with a second adhesive, wherein an elastic modulus the first adhesive is less than an elastic modulus of a second adhesive.

The present invention advantageously inhibits thermal strains in a substrate within an electronic structure, wherein such thermal strains result from thermal cycling operations on the electronic structure.

Please amend the paragraph beginning on page 3, line 9 and ending on page 5, line 3 as follows:

FIG.1 illustrates a front cross-sectional view of an electronic structure 10 using the same adhesive 21 in three different locations, in accordance with embodiments of the present invention. The adhesive may include, *inter alia*, silicone or epoxy. ~~Dow-Corning adhesive, identified as DC1-4173, may also be used as the adhesive.~~ The electronic structure 10 comprises a semiconductor device 37, a substrate 27, a stiffener ring 24, a thermally conductive cover plate 18, a heat sink 12, and the thermally conductive adhesive 21. The semiconductor device may include, *inter alia*, a semiconductor chip. The cover plate 18 may include, *inter alia*, nickel plated copper, and the heat sink 12 may include, *inter alia*, aluminum. The cover plate may have a thickness of at least about 20 mils. The substrate 27 has a compliance range of  $10^4$  psi to  $3 \times 10^6$  psi. The semiconductor device 37 is electrically coupled to a substrate 27 using a Controlled Collapse Chip Connection (C4) solder ball 42. The space surrounding the solder balls 42 may include an underfill 50. The substrate 27 may comprise, *inter alia*, a chip carrier or a printed circuit board. Input/Output (I/O) connections 29 may be attached to the substrate 27 such as when the substrate 27 is a chip carrier. The substrate 27 may include organic material such as, *inter alia*, TEFLON. A bottom surface 26 of the stiffener ring 24 is adhesively bonded to a top surface 34 of the substrate 27 such as by a tacky film adhesive. A bottom surface 22 of the cover plate 18 is adhesively coupled to both a top surface 23 of the semiconductor device 37 and a top surface 25 of the stiffener ring 24 by the adhesive 21. A bottom surface 14 of the heat sink 12 is adhesively coupled to a top surface 16 of the cover plate 18 by the adhesive 21. The adhesive 21 has a modulus of at least about 1000 psi (e.g., 1000-1200 psi). The coefficient of thermal

expansion (CTE) of the heat sink 12 (e.g., 10 ppm/°C to 24 ppm/°C) is greater than the CTE of the cover plate 18 (e.g., 10 ppm/°C to 24 ppm/°C). The CTE of the cover plate 18 is greater than the CTE of the semiconductor device 37 (e.g., 2 ppm/°C to 5 ppm/°C). The CTE of the semiconductor device 37 is less than the CTE of the substrate 27 (e.g., 8 ppm/°C to 50 ppm/°C). The difference between the aforementioned CTE's create stress on the substrate 27 during thermal cycling. If the adhesive 21 having a modulus of at least 1000 psi is used in the previously mentioned three locations, thermal cycling will cause the heat sink 12 to expand and express itself through the following: the adhesive 21 below the heat sink 12, the cover plate 18, and the next layer of adhesive 21 below the cover plate 18, ultimately stressing and constraining the semiconductor device 37. The thermal cycling will cause the substrate 27 to be stressed under the constrained semiconductor device 37. Since the semiconductor device 37 is constrained by the structure above as described *supra*, internal strain within the substrate 27 can cause fatigue with sufficient thermal cycling. This internal strain within the substrate 27 is primarily located at corners of the semiconductor device 37 footprint, the underfill 50, the C4 solder balls 42, and the substrate 27. As stated *supra*, the preceding problem is observed during thermal cycling. A solution to the previously mentioned problem is illustrated in FIG. 2.

Please amend the paragraph beginning on page 5, line 4 and ending on page 6, line 1 as follows:

FIG. 2 illustrates a modification of FIG. 1 using a combination three adhesives, in accordance with embodiments of the present invention. In FIG. 2, the electronic structure 10 uses an ultra low modulus adhesive 32 having a modulus of less than about 500 psi

and a thermal conductivity of at least about one watt per meter degree K to adhesively couple the top surface **23** of the semiconductor device **37** to the bottom surface **22** of the cover plate **18**. The ultra low modulus of the ultra low modulus adhesive **32** inhibits constraining of the semiconductor device and corresponding formation of strain on the substrate **27** during thermal cycling. A ~~[[T]] thermoset adhesive [[,]] identified as part number MG-120~~ can be used, *inter alia*, for the ultra low modulus adhesive **32**. For structural integrity, the adhesive **21**, used to adhesively couple the top surface **25** of the stiffener ring **24** to the bottom surface **22** of the cover plate **18** has a higher modulus than the ultra low modulus adhesive **32** used to adhesively couple the top surface **23** of the semiconductor device **37** to the bottom surface **22** of the cover plate **18**. An adhesive **15** is used to adhesively couple the bottom surface **14** of the heat sink **12** to the top surface **16** of the cover plate **18**. An advantage of using the ultra low modulus adhesive **32** to adhesively couple the top surface **23** of the semiconductor device **37** to the bottom surface **22** of the cover plate **18** is that the range of modulus for the adhesive **15** increases from 1000 - 1200 psi up to a value of about 1,000,000 psi. The adhesive **15** normally has a modulus that is less than the modulus of the adhesive **21**. However, the modulus of the adhesive **15** may or may not be equal to the modulus of the adhesive **32**, and still the advantage of the ultra-low modulus adhesive can be obtained.